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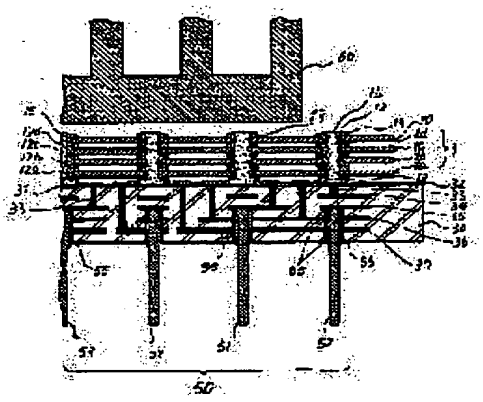
(54) ELECTRONIC PART MOUNTING STRUCTURE AND MANUFACTURE THEREOF

(57)Abstract:

PROBLEM TO BE SOLVED: To enable easy confirmation of an interconnected state between boards and also enable design modification of its design in a short time.

SOLUTION: An LSI chip is mounted to a film carrier 1. A plurality of such film carriers 1 are stacked on a wiring board 30. The film carriers 1 are provided therein with through holes 12. The adjacent film carriers 1 are connected by solder 15 filled in the respective through holes 12. An interconnected state of the through holes 12 can be confirmed by an appearance of the solder out of tope one of the through holes. When it is desired to modify its design, an additional film carrier is inserted between the film carriers 1.



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CLAIMS

[Claim(s)]
[Claim 1] Mounting structure of the electronic parts characterized by making pewter connection of those by which each adjoins in the direction of a laminating of said flexible substrate among said through holes of two or more of said flexible substrates including two or more flexible substrates which have a through hole, and by which the laminating was carried out.
[Claim 2] Mounting structure of the electronic parts according to claim 1 characterized by carrying said two or more flexible substrates in said 1st field of this wiring substrate, including further the wiring substrate which has a pad in the 1st field, and making pewter connection of said through hole of the lowest thing, and said pad of said wiring substrate among said two or more flexible substrates.
[Claim 3] Mounting structure of the electronic parts according to claim 1 characterized by filling up with the pewter in said through hole.
[Claim 4] Mounting structure of the electronic parts according to claim 1 characterized by carrying an electronic-circuitry chip in at least one of said the flexible substrates.
[Claim 5] Mounting structure of the electronic parts according to claim 1 characterized by arranging said through hole on the lattice point in each of two or more of said flexible substrates.
[Claim 6] Mounting structure of electronic parts according to claim 5 where this cutting means is characterized [in /, in at least one of said two or more of the flexible substrates / at least one of said the lattice points] by insulating between both sides of the flexible substrate concerned including a cutting means.
[Claim 7] Mounting structure of electronic parts according to claim 1 where at least one of said two or more of the flexible substrates is characterized by this connecting means connecting electrically between said at least two through holes on the flexible substrate concerned including a connecting means.
[Claim 8] It is the mounting structure of the electronic parts according to claim 5 characterized by connecting electrically the 2nd lattice point when said 1st lattice point and this 1st lattice point differ from each other while, as for said means for switching, at least one of said two or more of the flexible substrates insulates between both sides of the flexible substrate concerned in the 1st lattice point of said lattice points including a means for switching.
[Claim 9] Mounting structure of the electronic parts characterized by including the pewter which connects the 1st flexible substrate which has the 1st through hole, the 2nd flexible substrate which has said 1st through hole and the 2nd through hole which counters while a laminating is carried out to this 1st flexible substrate, and said the 1st through hole and said 2nd through hole.
[Claim 10] Mounting structure of the electronic parts according to claim 9 characterized by making pewter connection of said pad and said 1st through hole of said wiring substrate, including further the wiring substrate with which it has a pad in the 1st field, and said 1st flexible substrate is carried in this 1st field.
[Claim 11] In the manufacture approach of the mounting structure of the electronic parts containing the 1st flexible substrate which has the 1st through hole, and the 2nd flexible substrate which has the 2nd through hole The 1st step which positions a pewter on said 1st through hole, The 2nd step in which said

2nd flexible substrate is positioned so that said 2nd through hole may counter with said pewter, The manufacture approach of the mounting structure of the electronic parts characterized by including the 3rd step which dissolves said pewter, is made to move said some of pewters [at least] into said 2nd through hole, and connects said 1st and 2nd through holes with said pewter.

[Claim 12] In the manufacture approach of the mounting structure of the electronic parts containing the wiring substrate which has a pad, the 1st flexible substrate which has the 1st through hole, and the 2nd flexible substrate which has the 2nd through hole While regarding said 1st flexible substrate as the 1st step which positions a pewter on said pad of said wiring substrate so that said 1st through hole may counter said pewter The 2nd step in which said 2nd flexible substrate is positioned so that said 2nd through hole may counter said 1st through hole, Dissolve said pewter and said some of pewters [at least] are moved into said 1st and 2nd through holes. The manufacture approach of the mounting structure of the electronic parts characterized by including the 3rd step which connects said pad of said wiring substrate, said 1st through hole of said 1st flexible substrate, and said 2nd through hole of said 2nd flexible substrate with said pewter.

[Claim 13] In the manufacture approach of the mounting structure of the electronic parts containing the wiring substrate which has a pad, the 1st flexible substrate which has the 1st through hole, and the 2nd flexible substrate which has the 2nd through hole The 1st step which positions the 1st pewter on said pad of said wiring substrate, The 2nd step in which said 1st flexible substrate is positioned so that said 1st through hole may counter said 1st pewter, Dissolve said 1st pewter and said a part of 1st pewter [at least] is moved into said 1st through hole. The 3rd step which connects said pad of said wiring substrate, and said 1st through hole of said 1st flexible substrate with said 1st pewter, The 4th step which positions the 2nd pewter with the melting point lower than said 1st pewter on said 1st through hole, The 5th step in which said 2nd flexible substrate is positioned so that said 2nd through hole may counter said 2nd pewter, Dissolve said 2nd pewter at the temperature below the melting point of said 1st pewter, and said a part of 2nd pewter [at least] is moved into said 2nd through hole. The manufacture approach of the mounting structure of the electronic parts characterized by including the 6th step which connects said 1st and 2nd through holes with said 2nd pewter.

[Claim 14] It is. the manufacture approach of the mounting structure of the electronic parts for connecting two or more flexible substrates with which each has a through hole and by which the laminating was carried out — The 1st step which connects with a pewter those which adjoin in the direction of a laminating of said flexible substrate among the through holes of two or more of said flexible substrates, The manufacture approach of the mounting structure of the electronic parts characterized by including the 2nd step which checks the connection condition between said through holes when said pewter appeared in said through hole of the best thing among said two or more flexible substrates.

[Claim 15] Mounting structure of the electronic parts according to claim 1 characterized by including the radiator material thermally connected with mounting ****** electronic parts and these electronic parts at least among said two or more flexible substrates at the best thing, and the support means which supports this radiator material on said wiring substrate.

[Claim 16] Mounting structure of the electronic parts according to claim 1 characterized by said through hole having a taper.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[Field of the Invention] This invention relates to the mounting structure of electronic parts where the laminating of two or more substrates is carried out, especially about the mounting structure of electronic parts.
[0001]
[Description of the Prior Art] an example of the conventional technique of the mounting structure where the laminating of two or more substrates is carried out -- RAO R TSUMMARA, EUGEN Jay RIMASUTSUKI collaboration, and the "microelectronics packaging handbook" (Rao R.Tummala, Eugene J.Rymaszewski, "Microelectronics Packaging Hnadbook", 1989, Van Nostrand Reinhold, New York) of the 1989 fan NOSUTO land line HORUDO publication -- it is indicated by the 464th page from the 462nd page.
[0002] Reference of Fig. 7 [seven to] of this reference carries out the laminating of the two ceramic substrates with this technique. Between these ceramic substrates, it connects by soldering the pin projected from the inferior surface of tongue of an up substrate on the top face of a lower substrate.
[0003]
[Problem(s) to be Solved by the Invention] There were the following problems with this conventional technique.
[0004] It is hard to check the connection condition between substrates to the 1st. It is because a connection part is covered by the up substrate.
[0005] A design change takes [2nd] long duration. Compared with flexible substrates, such as a tape OUTOMEI Ted bonding (TAB) tape, it is for the design change of a ceramic substrate to require long duration. Specifically, the design change of a ceramic substrate takes several months to the design change of a TAB tape being completed in several days. The modification process of the mask of internal wiring or a screen requires especially time amount.
[0006] In view of the problem of such a conventional technique, the 1st purpose of this invention has the check of the connection condition between substrates in offering the mounting structure of easy electronic parts.
[0007] The 2nd purpose of this invention is to offer the mounting structure of the electronic parts which can carry out a design change for a short time.
[0008] The 3rd purpose of this invention is to shorten the connection wire length between electronic parts.
[0009]
[Means for Solving the Problem] Pewter connection of those by which the mounting structure of the electronic parts of this invention adjoins in the direction of a laminating of said flexible substrate among said through holes of two or more of said flexible substrates including two or more flexible substrates with which each has a through hole, and by which the laminating was carried out is made.
[0010] In the manufacture approach of the mounting structure of electronic parts where such a manufacture approach of mounting structure contains the 1st flexible substrate which has the 1st through hole, and the 2nd flexible substrate which has the 2nd through hole The 1st step which

positions a pewter on said 1st through hole, The 2nd step in which said 2nd flexible substrate is positioned so that said 2nd through hole may counter with said pewter, Said pewter is dissolved, said some of pewters [at least] are moved into said 2nd through hole, and the 3rd step which connects said 1st and 2nd through holes with said pewter is included.

[0011] It is. moreover, the manufacture approach of the mounting structure of electronic parts for other manufacture approaches to connect two or more flexible substrates with which each has a through hole and by which the laminating was carried out -- The 1st step which connects with a pewter those which adjoin in the direction of a laminating of said flexible substrate among the through holes of two or more of said flexible substrates, When said pewter appeared in said through hole of the best thing among said two or more flexible substrates, the 2nd step which checks the connection condition between said through holes is included.

[0012]

[Embodiment of the Invention] Next, the 1st example of this invention is explained with reference to a drawing.

[0013] When drawing 1 is referred to, the mounting structure of the electronic parts of the 1st example of this invention contains two or more tape carrier packages 1 by which the laminating was carried out to the top face of the wiring substrate 30 and the wiring substrate 30. Although the tape carrier packages 1a-1d of four layers are illustrated by drawing 1 , there is no constraint in the number of layers of a tape carrier package 1. Between the adjoining tape carrier packages 1, it connects according to the connection structure mentioned later. LSI chip 20 is mounted in the center section of each tape carrier package 1. The circuit side of LSI chip 20 is covered with plastics mold resin 22. The heat exchanger plate which is not illustrated intervenes between adjoining LSI chips 20. A heat exchanger plate is formed with right thermal-conductivity ingredients, such as a copper-tungsten alloy. Two or more I/O pins 50 are set up by the inferior surface of tongue of the wiring substrate 30.

[0014] When drawing 2 and drawing 3 are referred to, each tape carrier package 1 contains the flexible film 10. The ingredients of the flexible film 10 are insulating materials, such as polyimide resin and an epoxy resin. The flexible film 10 is **** about one-side the square of about 50mm. The flexible film 10 has the thickness of about 50 micrometers, and shows flexibility.

[0015] The device hole for holding LSI chip 20 is established in the center section of the flexible film 10. Two or more through holes 12 are arranged in the shape of a grid on the outside of a device hole. A lattice spacing is about 1.27mm. The diameter of a through hole 12 is about 100 micrometers. The land 13 which is a conductor pattern is formed in the perimeter and medial surface of a through hole 12. The diameter of a land 13 is about 300 micrometers.

[0016] A circuit pattern 11 is formed on the flexible film 10. The line breadth of a circuit pattern 11 is about 50 micrometers. The end of a circuit pattern 11 is connected to a through hole 12. The other end of a circuit pattern 11 is connected to the end of the beam lead 14 in the periphery of a device hole. The other end of the beam lead 14 is connected to a projection and the connection terminal of LSI chip 20 inside a device hole.

[0017] A tape OTOMEITIDDO bonding (TAB) technique can be used for manufacture of a tape carrier package 1, and mounting of LSI chip 20. the detail of a TAB technique -- for example, RAO R TSUMMARA, EUGEN Jay RIMASUTSUKI collaboration, and the "microelectronics packaging handbook" (Rao R.Tummala, Eugene J.Rymaszewski, "Microelectronics Packaging Hnadbook", 1989, Van Nostrand Reinhold, New York) of the 1989 fan NOSUTO land line HORUDO publication -- it is indicated by 409th page - the 454th page. The tape carrier package 1 manufactured with the TAB technique is called a TAB tape career.

[0018] The ingredient of the wiring substrate 30 is an epoxy resin, polyimide resin, etc. which were reinforced with the glass fiber. The wiring substrate 30 presents one-side the square of about 60mm. The wiring substrate 30 has the thickness of about 2.5mm, and shows strong rigidity. The wiring substrate 30 is a multilayer-interconnection substrate. The touch-down wiring layers 34 and 36 and the

power-source wiring layers 35 and 37 are formed in the interior of the wiring substrate 30.
[0019] Two or more pads 31 are formed in the top face of the wiring substrate 30. A pad 31 is arranged in the location corresponding to the through hole 12 of a tape carrier package 1. That is, a pad 31 is arranged in the shape of a grid. A lattice spacing is about 1.27mm. The solder resist 32 is covered by the field except the pad 31 of the top face of the wiring substrate 30.
[0020] Two or more I/O pins 50 are set up by the inferior surface of tongue of the wiring substrate 30. The I/O pin 50 is arranged in the shape of a grid. A lattice spacing is about 1.27mm. When mounting structure is mounted in a mother board, the I/O pin 50 is connected to this mother board. Since the I/O pin 50 has been arranged all over the inferior surface of tongue of the wiring substrate 30, the die length of wiring is made to the shortest using directly under [of LSI chip 20], or the I/O pin 50 of the near.
[0021] Reference of drawing 3 inserts the end of the I/O pin 50 in the hole 38 of the wiring substrate 30. The insulating coat 55 is covered by the insertion part of the I/O pin 50. A part of insulating coat 55 is removed, and the side face of the I/O pin 50 exposes it from this part. According to the removal part of the insulating coat 55, three sorts of I/O pins 51-53 are prepared. The upside insulating coat 55 is removed by the I/O pin 51. For this reason, the I/O pin 51 is connected to the power-source wiring layer 35. The lower insulating coat 55 is removed by the I/O pin 52. The I/O pin 52 is connected to the power-source wiring layer 37. The insulating coat 55 of pars intermedia is removed by the I/O pin 53. The I/O pin 53 is connected to the touch-down wiring layer 36. Thus, the internal wiring layer and the I/O pin 50 of the wiring substrate 30 are alternatively connectable with selection of a pin kind. Moreover, the through hole for signal pins is also established in the wiring substrate 30. A pin without pre-insulation is inserted in the through hole for signal pins.
[0022] Reference of drawing 2 and drawing 3 attaches the heat sink 60 for heat dissipation on LSI chip 20 mounted in the best tape carrier package 1d.
[0023] Next, the connection structure for tape carrier package 1a-1d is explained.
[0024] Reference of drawing 3 positions the tape carrier packages [1a-1d] through holes 12a-12d on a straight line on the pad 31 of the wiring substrate 30. These through holes 12a-12d are connected by the pewter 15. The through holes [12a-12d] interior is filled up with the pewter 15.
[0025] Next, the manufacture approach of the mounting structure of this example is explained with reference to a drawing. Specifically, how to carry out the laminating of the tape carrier packages 1a and 1b on the wiring substrate 30 is explained. By this laminating approach, two or more tape carrier packages 1 are connected at once.
[0026] Reference of drawing 4 (a) positions a pewter 15 on the pad 31 of the wiring substrate 30 in the 1st step. For example, the cream-like pewter 15 is printed on a pad 31.
[0027] Reference of drawing 4 (b) positions the tape carrier packages 1a and 1b by which the laminating was carried out on a pewter 15 in the 2nd step.
[0028] Reference of drawing 4 (c) heats a pewter 15 in the 3rd step. A pewter 15 dissolves and the part is sucked up inside through holes 12a and 12b. Then, a pewter 15 is cooled and through holes 12a and 12b are connected with a pad 31.
[0029] Next, other laminating approaches are explained. By this laminating approach, the laminating of the tape carrier package 1 is carried out one by one.
[0030] Reference of drawing 5 (a) positions pewter 15a on a pad 31 in the 1st step.
[0031] Reference of drawing 5 (b) connects through hole 12of tape carrier package 1a a to a pad 31 by drawing 4 (b) and the same approach as (c) in the 2nd step.
[0032] Reference of drawing 5 (c) positions pewter 15b on pewter 15a in the 3rd step. The melting point of pewter 15b is higher than the thing of pewter 15a.
[0033] Reference of drawing 5 (d) connects through hole 12of tape carrier package 1b b to through hole 12a by drawing 4 (b) and the same approach as (c) in the 4th step. Whenever [stoving temperature / of pewter 15b] is lower than the melting point of pewter 15a. For this reason, pewter 15a is not dissolved at the 4th step.

[0034] By the above manufacture approach, the connection condition of through holes 12a and 12b can be checked easily. What is necessary is just to specifically check that the pewter 15 has appeared inside the best through hole 12b. This can be checked only by viewing tape carrier package 1b from the upper part.
[0035] In the 1st example, one side of LSI chip 20 sets to 20mm, and the height which set LSI chip 20, a heat-conduction plate, and plastics mold resin 20 is set to 1mm. Supposing it supposes that a laminating is carried out at spacing whose LSI chip 20 is 2mm, it sets one side of a tape carrier package 1 to 50mm and four LSI chips 20 are mounted in one tape carrier package 1 16 LSI chips 20 are arranged in one-side 40mm and the field with a height of 4mm of the forward square pole. The wiring field of these LSI chips 20 becomes one-side 50mm and the forward square pole with a height of 4mm. Therefore, when LSI chip 20 interconnects with three-dimension direct system wiring, the wire length which connects between LSI chips 20 of the maximum ** is set to 104mm or less.
[0036] On the other hand, when 16 LSI chips 20 mentioned above are mounted in the substrate of one layer, the mounting field of LSI chip 20 serves as one-side a square of 80mm. In this structure, the wire length which connects LSI chip 20 comrades of the maximum ** amounts to about 160mm. Thus, according to this invention, the wire length between LSI chips 20 can be shortened.
[0037] Next, the 2nd example of this invention is explained with reference to a drawing. The description of the 2nd example is in the structure of a through hole 12. Other structures are the same as the 1st thing and essential target of an example.
[0038] Reference of drawing 6 forms the taper in the through hole 12 of the 2nd example.
[0039] Next, the 3rd example of this invention is explained with reference to a drawing. The description of the 2nd example is in the tape carrier package for design changes for making a design change easy. Other structures are the same as the 1st thing and essential target of an example. In the tape carrier package for design changes, a cutting means, a connecting means, and a means for switching are prepared suitably, and a design change is realized with the combination of these means.
[0040] Reference of drawing 7 (a) realizes the cutting means of the tape carrier package 4 for design changes by not preparing a through hole. As for the tape carrier package 1, the through hole 12 is formed on the lattice point. However, the tape carrier package 4 for design changes does not have a through hole on this lattice point, but it insulates between vertical sides. Instead of a through hole, a land 41 is formed in the top face of the tape carrier package 4 for design changes. Pewter connection of the land 41 is made in the through hole 12 of a tape carrier package 1. Thus, the signal through hole 33 and a through hole 12 are cut electrically. In addition, the ingredient of the flexible film 40 of the tape carrier package 4 for design changes, a dimension, and a configuration are the same as the thing of the flexible film 10, and good.
[0041] Reference of drawing 7 (b) realizes the connecting means of the tape carrier package 4 for design changes with the circuit pattern 43 prepared on the tape carrier package 4 for design changes. A circuit pattern 43 connects the through hole 421 and through hole 422 of the tape carrier package 4 for design changes. Thereby, the signal through hole 331 and the signal through hole 332 are connected.
[0042] Reference of drawing 7 (c) realizes the means for switching of the tape carrier package 4 for design changes in the combination of a cutting means and a connecting means. It has a tape carrier package 1 through hole 12 on the lattice point. However, the tape carrier package 4 for design changes does not have a through hole 12 at this lattice point. For this reason, a through hole 12 is cut as electrically as the signal through hole 331. Instead of a through hole, a land 44 is formed in the top face of the tape carrier package 4 for design changes. A land 44 is connected to a through hole 42 through a circuit pattern 43. A through hole 42 is located at lattice point when a through hole 12 is another. Thus, originally connection **** can make change-over connection of the through hole 12 of ** in the signal through hole 331 at the signal through hole 332.
[0043] It can respond to various design changes by combining a cutting means, a connecting means, and a means for switching. Compared with a multilayer-interconnection substrate, the tape carrier package 4

for design changes can be created in a short time. For this reason, the design change of the mounting structure can be carried out for a short time. Now, the tape carrier package 4 for design changes can be created in about two - three days.

[0044] In this example, the tape carrier package 4 for design changes was installed between the tape carrier packages 1 of the wiring substrate 30 and the lowest layer. However, it is also possible to install the tape carrier package 4 for design changes in other locations between layers. Moreover, two or more tape carrier packages 4 for design changes may be used.

[0045] Next, the 4th example of this invention is explained with reference to a drawing.

[0046] When drawing 8 is referred to, the description of this example is to have formed the supporter material 61 for supporting a heat sink 60. Other structures are the same as the 1st thing and essential target of an example.

[0047] The supporter material 61 has the column-like leg and Itabe prepared on this leg. The leg of the supporter material 61 is inserted in the hole established in the flexible film 10, and is fixed on the wiring substrate 30. At this time, LSI chip 20 of the best tape carrier package 1 and the inferior surface of tongue of Itabe of the supporter material 61 contact. Itabe has the hole in which the best through hole 12 is held. The electric contact to a through hole 12 and Itabe is prevented by this hole. A heat sink 60 is attached in the top face of the supporter material 61.

[0048] You may fill up with resin between the adjoining flexible films 10. Moreover, you may fill up with resin between the supporter material 61 and the best flexible film 10. As these resin, what combines insulation and right thermal conductivity is desirable.

[0049] With such structure, the heat generated from each LSI chip 20 gets across to best LSI chip 20 through the heat-conduction plate formed in the gap of LSI chip 20. The heat which got across to best LSI chip 20 gets across to a heat sink 60 through Itabe of the supporter material 61. The heat which got across to the heat sink 60 is exhausted by the open air.

[0050] In the 4th example, since a heat sink 60 is supported by the supporter material 61, the weight of a heat sink 60 does not join LSI chip 20. For this reason, even if it uses the large-sized heat sink 60, the dependability of LSI chip 20 does not fall. Moreover, the leg of the supporter material 61 functions also as a guide of a tape carrier package 1.

[0051] Next, other embodiments of this invention are explained.

[0052] Two or more LSI chips 20 may be mounted in one tape carrier package 1. The description of each above-mentioned example may be combined.

[0053]

[Effect of the Invention] As mentioned above, in this invention, LSI chip 20 was mounted in the tape carrier package 1, and the laminating of two or more tape carrier packages 1 was carried out. Between tape carrier packages 1, it connects by carrying out pewter attachment of the through hole 12 comrades prepared in the tape carrier package 1. A design change is realized by making the tape carrier package 4 for design changes intervene between tape carrier packages 1. The following effectiveness is attained by such configuration.

[0054] The connection condition between tape carrier packages 1 can check [1st] easily. What is necessary is just to specifically check visually that the pewter has appeared in the best through hole 12.

[0055] A design change is [2nd] possible for a short time. What is necessary is just to specifically insert the tape carrier package 4 for design changes. The tape carrier package 4 for design changes can be created in a short time.

[0056] To the 3rd, the connection wire length between electronic parts can be shortened. It is because electronic parts were mounted in three dimension.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] Drawing showing the structure of the 1st example of this invention.
[Drawing 2] The exploded view showing the structure of the 1st example of this invention.
[Drawing 3] Drawing showing the detailed structure of the 1st example of this invention.
[Drawing 4] Drawing showing the manufacture approach of the 1st example of this invention.
[Drawing 5] Drawing showing other manufacture approaches of the 1st example of this invention.
[Drawing 6] Drawing showing the structure of the through hole 12 of the 2nd example of this invention.
[Drawing 7] Drawing showing the structure of the tape carrier package 4 for design changes of the 3rd example of this invention.
[Drawing 8] Drawing showing the structure of the 4th example of this invention.
[Description of Notations]
1, 1a-1d Tape carrier package
10, 10a-10d Flexible film
11 Circuit Pattern
12, 12a-12d Through hole
121 Through Hole
122 Through Hole
13 Land
14 Beam Lead
15 Pewter
20 LSI Chip
22 Plastics Mold Resin
30 Wiring Substrate
31 Pad
32 Solder Resist
33 Signal through Hole
331 Signal through Hole
332 Signal through Hole
34 Touch-down Wiring Layer
35 Power-Source Wiring Layer
36 Touch-down Wiring Layer
37 Power-Source Wiring Layer
38 Hole
4 Tape Carrier Package for Design Changes
40 Flexible Film
41 Land
42 Through Hole
421 Through Hole
422 Through Hole

43 Circuit Pattern
44 Land
50 I/O Pin
51 I/O Pin
52 I/O Pin
53 I/O Pin
55 Insulating Coat
60 Heat Sink
61 Supporter Material

[Translation done.]

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